ABSTRACT OF THE DISCLOSURE

An access circuit for efficiently accessing a buffer memory in accordance with an instruction from an external circuit. An access data unit for accessing a SDRAM in one operation clock cycle of the access circuit may be switched between one byte, one word, and two words. The switching of the access data unit is performed in accordance with a data unit designation signal generated by decoding address data, which is provided to a control unit, with an address decoder. The memory interface receives a request signal that is in accordance with the data unit designation signal from a request generator and accesses the buffer memory in the access data unit that is in accordance with the request signal.